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Patentanmeldung Nr. Patent application No. Demande de brevet n°

04100300.5

Der Präsident des Europäischen Patentamts;
Im Auftrag

For the President of the European Patent Office

Le Président de l'Office européen des brevets
p.o.

R C van Dijk

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(Falls die Bezeichnung der Erfindung nicht angegeben ist, siehe Beschreibung.
If no title is shown please refer to the description.
Si aucun titre n'est indiqué se referer à la description.)

Integrated circuit device with a ROM matrix

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Integrated circuit device with a ROM matrix

The invention relates to an integrated circuit device with a ROM (Read Only Memory) matrix.

US patent No. 5,930,180 discloses a ROM (Read Only Memory) matrix with a sense amplifier that contains a pair of cross coupled inverters. The input of one of the inverters is coupled to a bit line and the input of the other inverter is coupled to a reference bit line. The pair of cross coupled inverters acts as a differential sense amplifier, which eventually assumes one logical state or another, dependent on the values of the voltages on the bit line and the reference bit line when the inverters are activated.

Differential sensing has obvious advantages in terms of speed and sensitivity, which translates into the capacity to work with a large ROM matrix. However, for reliable differential sensing of single ended signals a reference signal is required. This is the case in conventional ROMs, in which each data bit is represented by the absence or presence of a single circuit connection that determines whether or not a memory cell pulls down the voltage on a bit line if the memory cell is selected.

US patent No. 5,930,180 uses a reference bit line to generate the reference signal. One reference bit line is provided for a plurality of normal bit lines. In ROMs the speed of initial signal development on the bit lines depends much more heavily on unselected data than in DRAMs or SRAMs. The data in unselected memory cells, which is expressed by the absence or presence of circuit connections to the bit lines and/or the word lines, affects the capacitive load on the bit lines and/or word lines. Thus, different bit lines will have different capacitive load value. The reference bit line, which has to serve as a reference for any selected bit line, can only provide one capacitive load value. As a result careful matching is needed to ensure that the voltage on the reference bit line can be used to distinguish between different data values. This leaves a small margin of error. However, the voltage on the reference bit line can easily be disturbed by interference. Moreover the reference bit line takes up place in the integrated circuit and its operation consumes power.

Among others, it is an object of the invention to provide for an integrated circuit device that contains a read only memory matrix with a differential sense amplifier in which no capacitance balancing is needed between the bit line that is coupled to one differential input of the sense amplifier and a reference circuit coupled to another differential input.

Among others, it is an object of the invention to provide for an integrated circuit device that contains a read only memory matrix with a differential sense amplifier in which no reference bit line is needed that supplies a reference voltage to the differential sense amplifier.

The invention provides for an integrated circuit device according to Claim 1. The device contains a read only memory with a differential sense amplifier. The sense amplifier is used in a two phase read out process, wherein first a charge sharing connection is established between a selected bit line and a first input node of the sense amplifier and in a second phase the charge sharing connection is severed and amplification of the sense amplifier is activated. A reference circuit drives a reference voltage to a second input node of the sense amplifier, but driving is interrupted in the second phase. Thus the sense amplifier amplifies only once its inputs are no longer coupled to the bit line and driven by the reference circuit. As a result no capacitance balancing between the bit line and the reference circuit is needed. Therefore, the reference circuit may be included in the periphery of the memory matrix, without using a reference bit line that extends along the entire memory matrix in parallel with the bit lines.

The timing circuit preferably comprises a dummy bit line that generates a dummy bit signal with the slowest possible signal development that may occur on any bit line. The timing circuit is arranged to switch to the second phase only when this dummy bit signal reaches a threshold, that has been selected so that it is ensured that the potential on any active bit line will have crossed the reference voltage when the dummy bit signal reaches the threshold.

In an embodiment the differential sense amplifier has a first and second switching circuit coupled between the sense amplifier and the first and second power supply connection respectively, the timing circuit deactivating and activating amplification by the sense amplifier by making both switching circuits non-conductive and conductive respectively. Thus the sense amplifier cannot amplify any signals as long as the bit line is coupled to the sense amplifier. The sense amplifier may comprise a pair of cross coupled

inverters for example, such a positive feedback circuit will eventually assume one of two defined states dependent on the charge received from the bit line.

These and other objects and advantageous aspects of the invention will be described by way of example using the following figures

Figure 1 shows a read only memory circuit

Figure 1a shows two bit-lines

Figure 1b shows a timing circuit

Figure 2 shows a sense amplifier

Figure 3 shows a reference circuit

Figure 3a shows an alternative reference circuit

Figure 4 shows timing signals

Figure 1 shows a read only memory circuit, comprising a memory matrix 10, a column precharge circuit 12, an addressing circuit 14a, 14b, a column multiplexer 16, sense amplifiers 18, and a timing circuit 19.

Figure 1a shows part of memory matrix 10 and precharge circuit 12 in more detail. The memory matrix is organized in rows and columns. The memory matrix comprises a plurality of bit lines 102 (only two shown), each corresponding to a respective column. The precharge circuit comprises precharge transistors 120 each with a main current channel coupled between a respective bit line 102 and a first power supply connection Vdd. The control electrodes of precharge transistors 120 are connected together and to a precharge input.

The memory matrix comprises a plurality of word lines WL0, WL1, WL2…, each corresponding to a respective one of the rows. Each cross point of a bit line 102, and a word line WL0, WL1, WL2,.. corresponds to a memory cell. Data is represented by the presence or absence of data transistors 100, with a main current channel coupled between the bit line 102 and a second power supply connection (Vss not shown explicitly). The control electrodes of each particular data transistor 100 is coupled to the word line WL0, WL1, WL2, … of the row to which the particular data transistor 100 belongs. By way of example a first bit line 102 is connected to data transistors 100 that have control electrodes coupled to word lines WL0, WL2, etc. but not to a data transistor 100 that has a control electrode coupled to

word line WL1. A second bit line 102 has no data transistor 100 that has a control electrode coupled to word line WL1. It will be appreciated that the data that is stored determines exactly which bit lines are coupled to data transistors 100 that are connected to respective word lines WL0, WL1, WL2... in memory matrix 10.

Figure 1b shows an example of a timing circuit 19. Part of this timing circuit geographically forms part of memory matrix 10. This part contains a dummy bit line 194, connected to the first power supply connection Vdd via the main current channel of one of the precharge transistors 120 of precharge circuit 12. At the positions that correspond to rows reference transistors 190 are coupled to dummy bit line 194. Reference transistors 190 are identical to the data transistors of memory matrix 10, however, their control electrodes are coupled to the second power supply connection Vss, so that the main current channels of reference transistors 190 are non conductive.

The timing circuit also contains a pulse generator circuit 196 and a dummy data transistor 192. Dummy data transistor 192 is coupled to dummy bit line similarly to the data transistors of memory matrix 10, but its control electrode is driven by pulse generator 196. Dummy bit line 194 is coupled to an input of pulse generator 196.

The timing circuit is arranged to generate pulses with a width that corresponds to a worst case time needed to lower the potential of any of the bit lines 102 where one data transistor 100 conducts below a threshold voltage. This realized by applying a signal transitions at the start of a pulse to the control electrode of dummy data transistor 192 and using the resulting voltage change on dummy bit line 194 to terminate the pulse. A conventional inverter circuit, with an input coupled to dummy bit line 194 may be used to signal when to end the pulse for example. To ensure sufficient width dummy bit line 194 preferably is capacitively loaded with the maximum number of transistors (reference transistors 190 and dummy data transistor 192) that can load a real bit line (one for each row), however, it should be appreciated that small deviations from this number do not significantly affect the timing circuit.

Preferably, timing circuit 19 also contains a structure that affects transfer of the voltage from dummy bit line to the thresholding in the same way as column multiplexer 16 does for the bit lines.

Addressing circuit 14a, 14b comprises a row selector 14a, which receives a first part of a memory address and has outputs coupled word lines WL0, WL1, WL2.... Furthermore, addressing circuit 14a, 14b comprises a column multiplexer 16 which couples a

set of selected bit lines to sense amplifiers 18, selected under control of a second part of the memory address.

Figure 2 shows a sense amplifier circuit. At the heart of the sense amplifier is a pair of inverter circuits (244a, 244b), (246a, 246b) with cross-coupled inputs and outputs and with interruptible power supply connections to both the first and the second power supply connection Vdd, Vss.

A first power supply transistor 240 has a main current channel coupled between the first power supply Vdd and a first node 241. Each comprising a series connection of the main current channel of a PMOS transistor 244a, 246a, and an NMOS transistor 244b, 246b, both coupled between the first node 241 and a second node 243. The second node 243 is coupled to the second power supply Vdd via the main current channel of a second power supply transistor 242. The control electrodes of the PMOS transistor 244a, 246a and the NMOS transistor 244b, 246b of each series connection are coupled to each other and to a node between the main current channels of the transistors of the other series connection.

The sense amplifier circuit contains an NMOS transistor 20a and a PMOS transistor 20b with their main current channels coupled in parallel between an output of column multiplexer 16 and an internal bit line part BL, which is coupled to the input of a first one (246a, 246b) of the pair of inverters. Furthermore the sense amplifier circuit contains a reference circuit 22 with an output REF coupled to the input of a second one (244a, 244b) of the pair of inverters.

Figure 3 shows an embodiment of reference circuit 22. This reference circuit contains equalization transistors 30, 32, 34 with main current channels coupled between internal bit line part BL and the first power supply connection Vdd, internal bit line part BL and the reference output REF, and the reference output REF and the first power supply connection Vdd respectively. The control electrodes of the equalization transistors are coupled together. Furthermore, reference circuit 22 comprises an NMOS bias transistor 36 and a PMOS bias transistor 38, having main current channels coupled between the reference output REF and the first power supply connection Vdd and the reference output REF and the second power supply connection Vss respectively.

Figure 4 will be used to illustrate the operation of the read only memory circuit. Operation is initiated by processing circuits (not shown) that supply addresses to the address inputs of addressing circuits 14a, 14b and read data from sense amplifiers 18, synchronizing their operation with that of the memory circuit by means of a clock signal

CLK. Operation of the memory circuit starts upon reception of a transition 40 in the clock signal CLK that is supplied to timing circuit 19.

Prior to transition 40 the memory is in a preliminary phase of operation. In this phase precharge transistors 120 in precharge circuit 12 couple the bit lines to the first power supply connection, so that their potential is drawn to Vdd. NMOS transistor 20a and a PMOS transistor 20b are non conductive. Equalization transistors 30, 32, 34 are conductive, so that the potentials on internal bit line part BL and reference output REF are equalized and drawn to Vdd. First and second power supply transistors 240, 242 are non-conductive.

Transition 40 triggers a first phase of operation of the memory. In response to transition 40 in a clock signal CLK timing circuit 19 generates a first transition 41 in a decode signal DEC and its logic complement DECn. DEC is supplied to precharge circuit 12 to cause the main current channels of precharge transistors 120 to become non-conductive in the first phase. With a slight delay with respect to DEC, a signal DEC' generated by timing circuit 19 causes row selector 14a to raise the voltage on an addressed one of the word lines WL0, WL1, WL2, ...

As a result the voltage on the bit lines 102 that contain a data transistor 100 in the selected row (as indicated by the word lines) will be pulled down by the relevant data transistors 100. This is illustrated by the solid line in the signal A of the figure. The voltage on the bit lines 102 that do not contain a data transistor 100 in the selected row generally also drops, due to leakage currents, but more slowly than if a data transistor 100 is present. This is illustrated by the dashed line in signal A of the figure.

Column multiplexer 16 conductively couples selected ones of the bit lines to sense amplifiers 1. In the sense amplifiers 1 equalization transistors 30, 32, 34 are made non conductive in the first phase upon transition 40 of the clock signal CLK. Under control of the DEC and DECn signals NMOS transistor 20a and PMOS transistor 20b are made conductive. As a result the selected bit lines 102 share charge with the internal bit line parts BL. Therefore the potential of the internal bit line part BL follows the potential of a selected bit line 102 in the first phase.

In the first phase NMOS and PMOS bias transistors 36, 38 are made conductive under control of DEC and DECn. As a result the reference output REF assumes a potential determined by these bias transistors. This potential is roughly one threshold voltage VTn of NMOS bias transistor 36 below the potential of the first power supply connection Vdd. Because the source of NMOS bias transistor 36 is not at Vdd potential the threshold VTn is higher than for normal NMOS transistors of the integrated circuit, that have their

source connected to Vdd. Bias transistors 36, 38 are dimensioned so that the voltage at the reference output REF is higher than the threshold voltage at dummy bit line 194 at which timing circuit 19 cuts off the DEC pulse. Thus, it is ensured that the potential on even the most loaded bit line that is pulled down by a data transistor 100 will have dropped below the reference voltage at the end of the DEC pulse. It should be noted that the speed with which the reference output REF assumes its reference level is generally much faster than the speed of potential change of bit line part BL, because reference output REF is not loaded by a bit line to which many data transistors may be connected and because the control electrodes of bias transistors 36, 38 are driven directly by DEC and DECn.

A second phase of operation starts in response to a second transition 42 in the decode signal DEC. Timing circuit 19 generates second transition 42 with a delay after first transition 41. The delay is determined by the time interval needed to discharge dummy bit line 194 so that the potential of dummy bit line 194 drops below a threshold value. Because of the construction of timing circuit 19 it is ensured that this time interval is larger than the time interval needed by any of the bit lines 102 to reach the threshold value if a selected data transistor 100 is connect to that bit line 102.

In the second phase the conductive connection between the selected bit lines 102 and the bit line parts BL is severed (by making pass transistors 20a,b non-conductive) and the bias transistors 36, 38 are made non-conductive. Subsequently first and second internal power supply nodes 241, 243 of the cross coupled inverters (244a, 244b), (246a,246b) of the sense amplifiers are coupled to the power supply connections Vdd, Vss.

As a result the cross coupled inverters (244a, 244b), (246a,246b) amplify any potential difference between their inputs, i.e. bit line part BL and reference output REF until a state is assumed wherein one inverter has a logic low input and the other a logic high. These logic levels are used as output signals. These levels may be latched into a latch circuit (not shown; e.g. a pair of NAND gates, each with a first input coupled to the output of a respective one of the inverters and a second input coupled to the output of the other NAND gate). From this latch circuit the data is supplied to the processing circuits (not shown for further use).

Once that data has been latched the circuit is ready for a next cycle. This cycle may be started by another transition 44 in clock signal CLK, upon which the circuit returns to the preliminary phase of operation.

Thus, by preventing that the sense amplifier provides active amplification while a selected bit line shares charge with internal bit line part BL, and severing the

connection between the selected bit line 102 and the internal bit line part BL prior to active amplification it, is made possible that a differential sense amplifier can be used with a reference circuit that does not need to have capacitive characteristics similar to those of the bit lines. In particular, a reference circuit can be used that does not contain a dummy bit line that extends in parallel with the bit lines of memory matrix 10 to provide a reference voltage. Thus, potential interference problems due to the such a dummy bit line are eliminated, and space and power consumption for generating the reference voltage are reduced.

Because the reference circuit doe requires only a few transistors, the reference circuit does not significantly suffer from leakage currents. This makes it easier to ensure a proper reference level.

Fig.3a shows an alternative embodiment of reference circuit 22. Compared to figure 3, in this embodiment bias transistors 36, 38 have been replaced by an alternative bias circuit, containing a PMOS bias transistor 360, an NMOS bias transistor 380, and a first and second PMOS control transistor 390, 395. Reference output REF is coupled to first power supply connection Vdd via the main current channel of PMOS bias transistor 360 and to second power supply connection Vss via the main current channel of NMOS bias transistor 380. The main current channel of first control transistor 390 is coupled between reference output REF and the control electrode of PMOS bias transistor 380. The control electrode of first control transistor 390 receives DECn. The main current channel of second control transistor 390 is coupled between the control electrode of PMOS bias transistor 380 and first power supply connection Vdd. The control electrode of second control transistor 390 receives DEC.

In operation, in the first phase NMOS bias transistor 380 is made conductive under control of DEC. First PMOS control transistor 390 is made conductive as well. As a result, PMOS bias transistor 360 operates as a diode, the circuit generating a reference level determined by the voltage drop across PMOS bias transistor 360 under influence of the current through NMOS bias transistor 380. Bias transistors 36, 38 are dimensioned so that the voltage at the reference output REF is higher than the threshold voltage at dummy bit line 194 at which timing circuit 19 cuts off the DEC pulse. Thus, it is ensured that the potential on even the most loaded bit line that is pulled down by a data transistor 100 will have dropped below the reference voltage at the end of the DEC pulse. Outside the first phase, second control PMOS transistor 395 is made conductive to ensure that PMOS bias transistor 360 becomes non-conductive.

It should be appreciated that the invention is not limited to the particular embodiments sense amplifier circuit or the reference circuit shown in the figures. Other, known reference voltage generating circuits may be used. Such a reference circuit could permanently generate a reference voltage and be connected to the reference output via one or more pass transistors similar to pass transistors 20a,b. In this case these pass transistors could be made conductive under control of the DEC pulse for example. Similarly, other amplifiers could be used that are initialized to a balanced state prior to sensing and activated after the connection between the selected bit line and the bit line segment BL has been severed and the reference output REF also has become floating.

Similarly, it should be realized that other types of ROM matrix may be used, for example data transistors may be present at all cross points between word lines and bit lines, but only selected ones may be connected to the bit lines, for example by fuse blowing or mask programming. Similarly a ROM matrix may be used in which the data transistors are all coupled to the bit lines, but only some are coupled to the word lines. Such a coupling may be mediated by a floating gate. Similarly, ROMs using any way of programming may be used, such as for example late programmable ROM's (metal), ROMs that are programmed by adding contact holes or not etc.

CLAIMS:

1. An integrated circuit device, comprising

- a read only memory matrix (10), comprising cells organized in columns with associated bit lines (102) and rows with associated word lines (WL), the matrix (10) comprising data transistors (100) coupled to both the bit lines (102) and the word lines (WL) in data dependent ones of the cells;

- a differential sense amplifier (18), having a first input (BL), a second input (REF), and a control input (SNS, SNSn) for controlling activation and deactivation of amplification by the sense amplifier (18);

- a coupling circuit (16) coupled between the bit lines (102) and the first input (BL), for controllably permitting charge sharing between a selectable one of the bit lines (102) and the first input (BL);

- a reference circuit (22) coupled to the second input (REF), and arranged to controllably activate driving of a reference voltage at the second input (REF);

- a timing circuit (19) arranged to signal operation in a first phase, when the word lines (WL) have selected a row of the matrix, followed by a second phase, the timing circuit (19) controlling the coupling circuit (16) to permit charge sharing between the input and the selectable one of the bit lines (102) in the first phase, and the timing circuit (19) in the second phase controlling the coupling circuit (16) to prevent said charge sharing, making the reference circuit (22) deactivate driving the reference voltage, and activating amplification by the differential sense amplifier (18) only when said charge sharing has been prevented and said driving has been deactivated.

2. An integrated circuit device according to Claim 1, wherein the timing circuit (19) comprises

- a dummy bit line(194) capacitively loaded substantially as capacitive loading of a hypothetical bit line (102) with a maximum number of data transistors (100) coupled to that hypothetical bit line (102);

- a dummy data transistor (192) coupled to the dummy bit line (194);

- a trigger circuit (196) for triggering the second phase, the trigger circuit (196) activating the dummy data transistor (192) in the first phase and starting the second phase when a potential swing on the dummy bit line (194) due activation of the dummy data transistor (192) in the first phase exceeds a threshold value larger than a potential swing that is needed on the bit line (102) to cross the reference voltage.

3. An integrated circuit device according to Claim 1, wherein the reference circuit (22) is local to a periphery of the memory matrix (10), without containing signal lines that extend in parallel with the bit lines (102) over a column height of the matrix (10).

4. An integrated circuit device according to Claim 1, wherein the differential sense amplifier (18) is connected between a first and second power supply connection (Vss, Vdd), the sense amplifier (18) comprising s first and second switching circuit (240, 242) coupled between the sense amplifier (18) and the first and second power supply connection respectively (Vdd, Vss), the timing circuit (19) deactivating and activating amplification by the sense amplifier (18) by making both switching circuits (240, 242) non-conductive and conductive respectively.

5. An integrated circuit device according to Claim 4, wherein the differential sense amplifier (18) comprises a pair of inverters (244ab, 246ab), with inputs coupled to the first and second input (BL, REF) respectively and outputs cross coupled to each others inputs, the inverters (244ab, 246ab) receiving power supply from the power supply connections (Vdd, Vss) via the first and second switching circuit (240, 242).

6. An integrated circuit device according to Claim 5, comprising a latch circuit having inputs coupled to the outputs of the inverters (244ab, 246ab).

7. An integrated circuit device according to Claim 1, wherein the reference circuit (22) comprises a controllable equalization circuit (30, 32, 34) coupled between the first and second input (BL, REF), and arranged to equalize potentials on said first and second input (BL, REF) prior to said first phase.

8. An integrated circuit device according to Claim 1, wherein the reference circuit comprises a PMOS bias transistor (38) and an NMOS bias transistor (36) with a main

current channel coupled from the second input (REF) to a negative and a positive power supply terminal (Vss, Vdd) respectively, the timing circuit being arranged to drive the control electrodes of the PMOS bias transistor (38) and the NMOS bias (36) transistor to the potential of the negative and positive power supply terminal (Vss, Vdd) respectively during said first phase.

9. An integrated circuit device according to Claim 1, wherein the reference circuit comprises an first bias transistor (38) and a second bias transistor (36) of mutually opposite polarity with a main current channel coupled to respective power supply terminals (Vss, Vdd), the timing circuit (19) being arranged to switch the main current channel of the first bias transistor (38) to a conductive state and to switch the second bias transistor (36) as a diode during said first phase.

10. An integrated circuit device according to Claim 1, wherein the timing circuit comprises

- a dummy bit line (194) with a capacitive load substantially corresponding to a maximum possible capacitive load for any of the bit lines (102),
- a pull transistor (192) for pulling the potential of the dummy bit line starting from a the start of the first phase;
- a trigger circuit (196) for triggering the second phase when the potential swing due to said pulling exceeds a threshold value larger than a potential swing that is needed on the bit line (102) to cross the reference voltage.

11. An integrated circuit device according to Claim 1, comprising a precharge circuit (120) arranged to precharge the bit lines from a first power supply connection (Vdd) prior to said first phase and to decouple the bit lines (102) from the first power supply connection (Vdd) during said second phase.

12. A method of reading data from a read only memory matrix in an integrated circuit device, the read only memory matrix (10) comprising cells organized in columns with associated bit lines (102) and rows with associated word lines (WL), the matrix (10) comprising data transistors (100) coupled to both the bit lines (102) and the word lines (WL) in data dependent ones of the cells;

- providing a differential sense amplifier (18), having a first input (BL), a second input (REF), and a control input (SNS, SNSn) for controlling activation and deactivation of amplification by the sense amplifier (18);
- providing a coupling circuit (16) coupled between the bit lines (102) and the first input (BL), for controllably permitting charge sharing between a selectable one of the bit lines (102) and the first input (BL);
- providing a reference circuit (22) coupled to the second input (REF), the method comprising the following steps
- controllably activating the reference circuit to drive a reference voltage at the second input (REF);
- signalling operation in a first phase, when the word lines (WL) have selected a row of the matrix, wherein the coupling circuit (16) is controlled to permit charge sharing between the input and the selectable one of the bit lines (102), followed by a second phase, wherein the coupling circuit (16) is controlled to prevent said charge sharing, making the reference circuit (22) deactivate driving the reference voltage, and activating amplification by the differential sense amplifier (18) only when said charge sharing has been prevented and said driving has been deactivated.

ABSTRACT:

A read only memory matrix in an integrated circuit contains data transistors coupled to both the bit lines and the word lines in data dependent ones of the cells of the matrix. A differential sense amplifier has a first input coupled to a bit line, a second input coupled to a reference circuit and a control input for controlling activation and deactivation of amplification by the sense amplifier. A coupling circuit controllably permits charge sharing between a selectable one of the bit lines and the first input. A timing circuit is arranged to signal operation in a first phase, when the word lines have selected a row of the matrix, followed by a second phase. The timing circuit controls the coupling circuit to permit charge sharing between the input and the selectable one of the bit lines in the first phase. In the second phase the timing circuit controls the coupling circuit to prevent charge sharing, makes the reference circuit deactivate driving the reference voltage, and subsequently activates amplification by the differential sense amplifier. Preferably the timing circuit contains a dummy bit line and a trigger circuit for triggering the second phase when a potential swing on the dummy bit line exceeds a threshold value.

Fig. 1

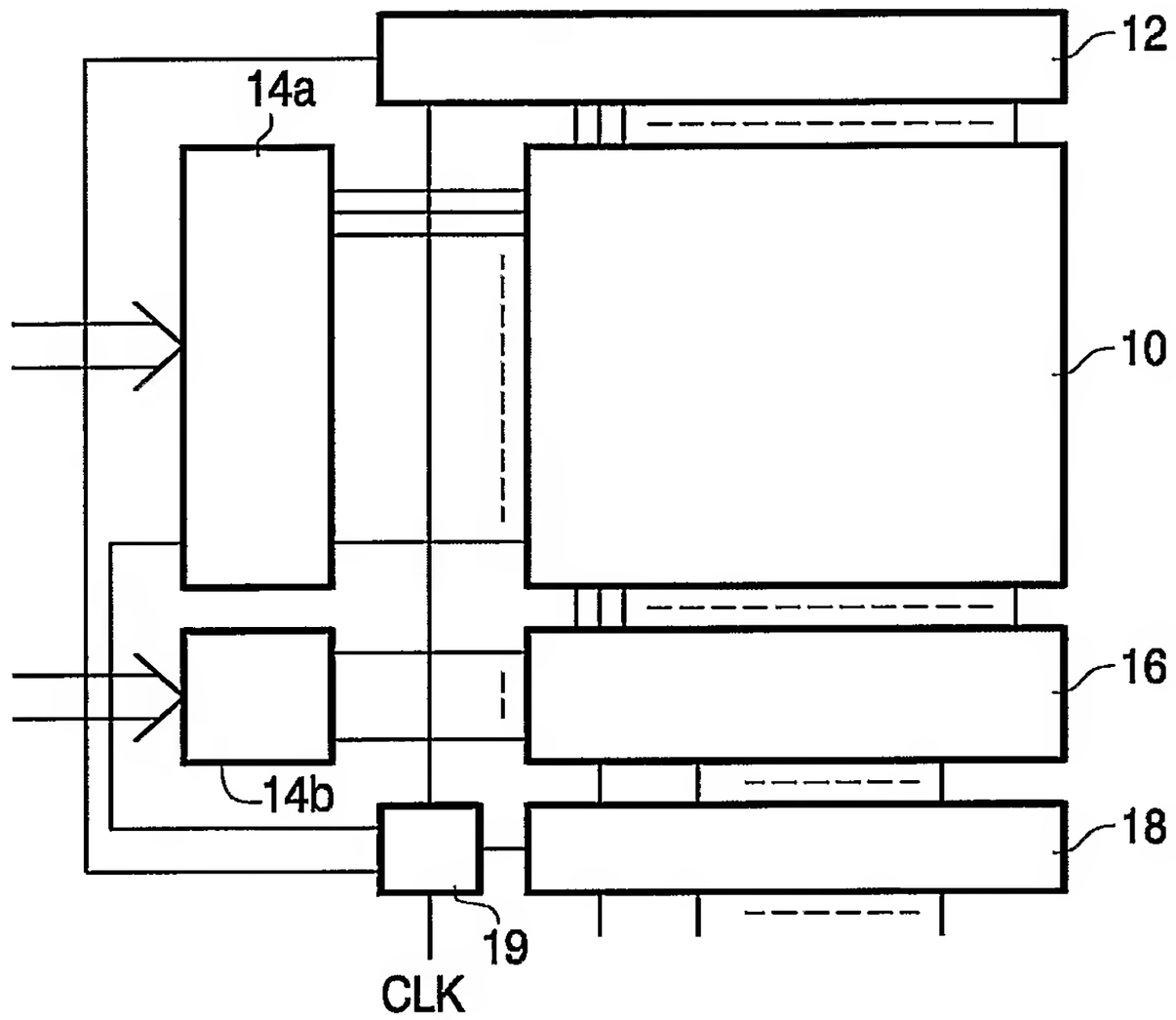
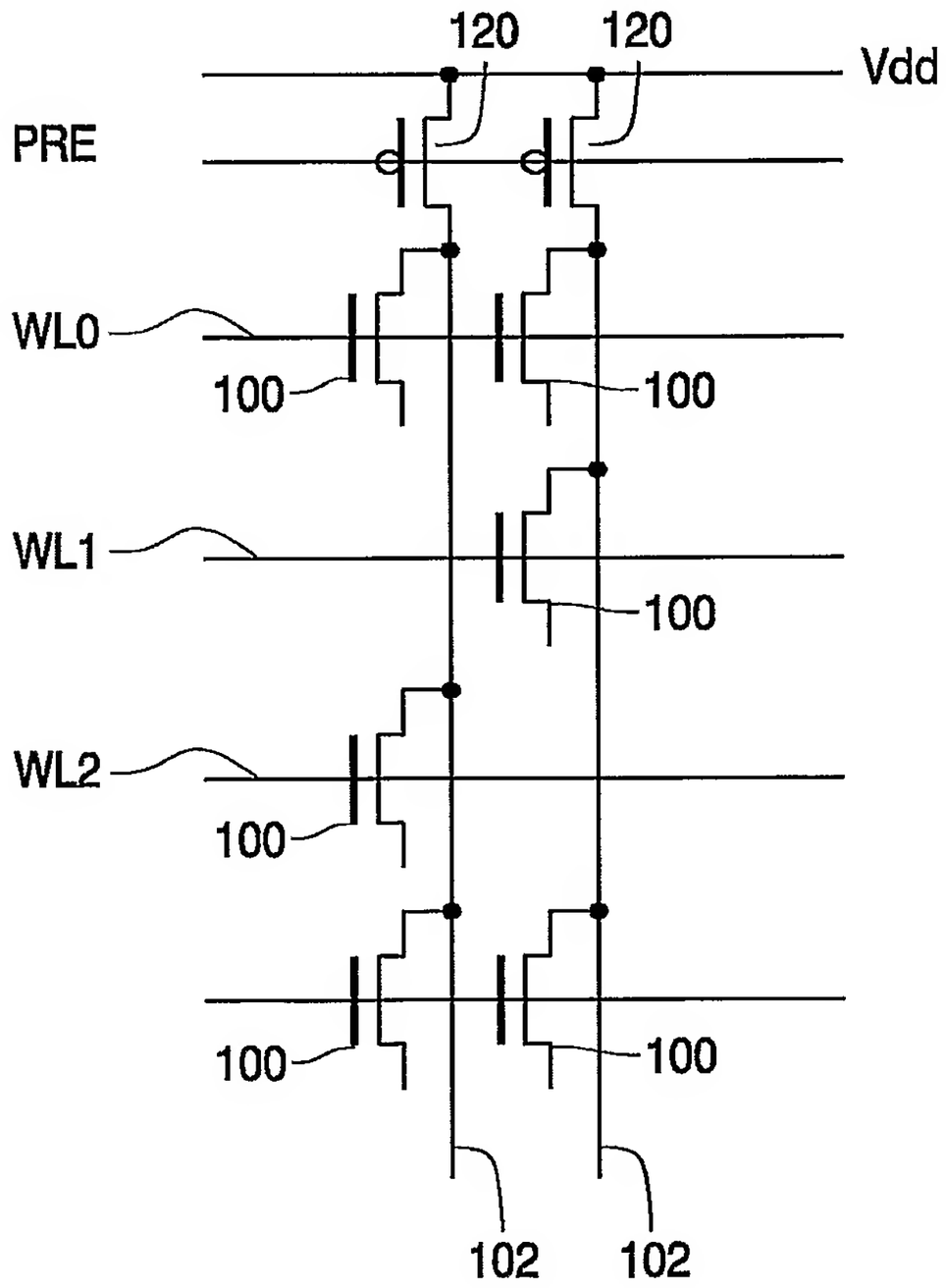

12
14a
10
16
14b
18
19
CLK

FIG. 1


120
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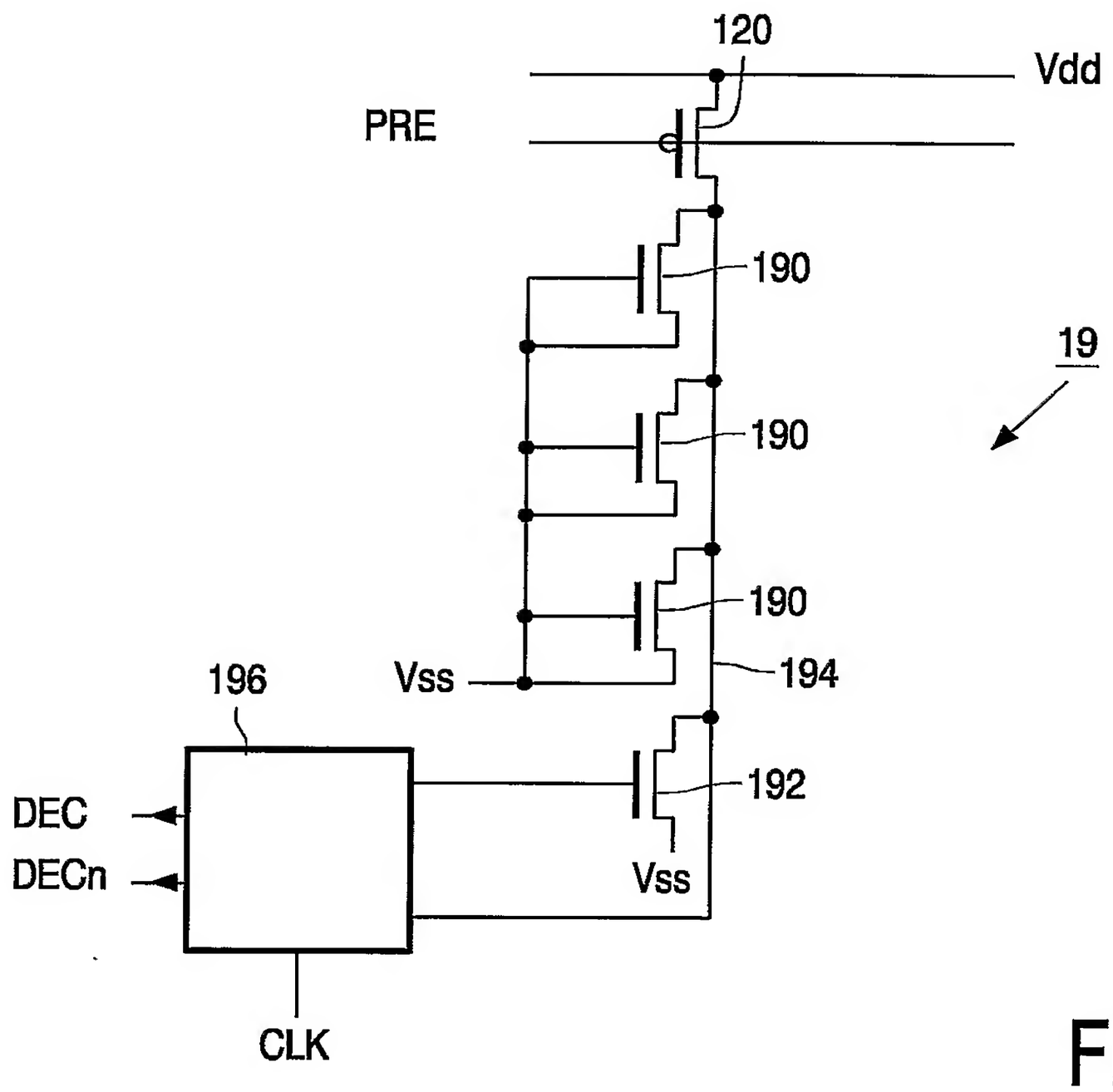
Vdd
PRE
WL0
100
100
WL1
100
WL2
100
100
100
102
102

FIG. 1a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Vdd
PRE
190
19
190
190
196
Vss
194
192
DEC
DECn
Vss
CLK

FIG. 1b

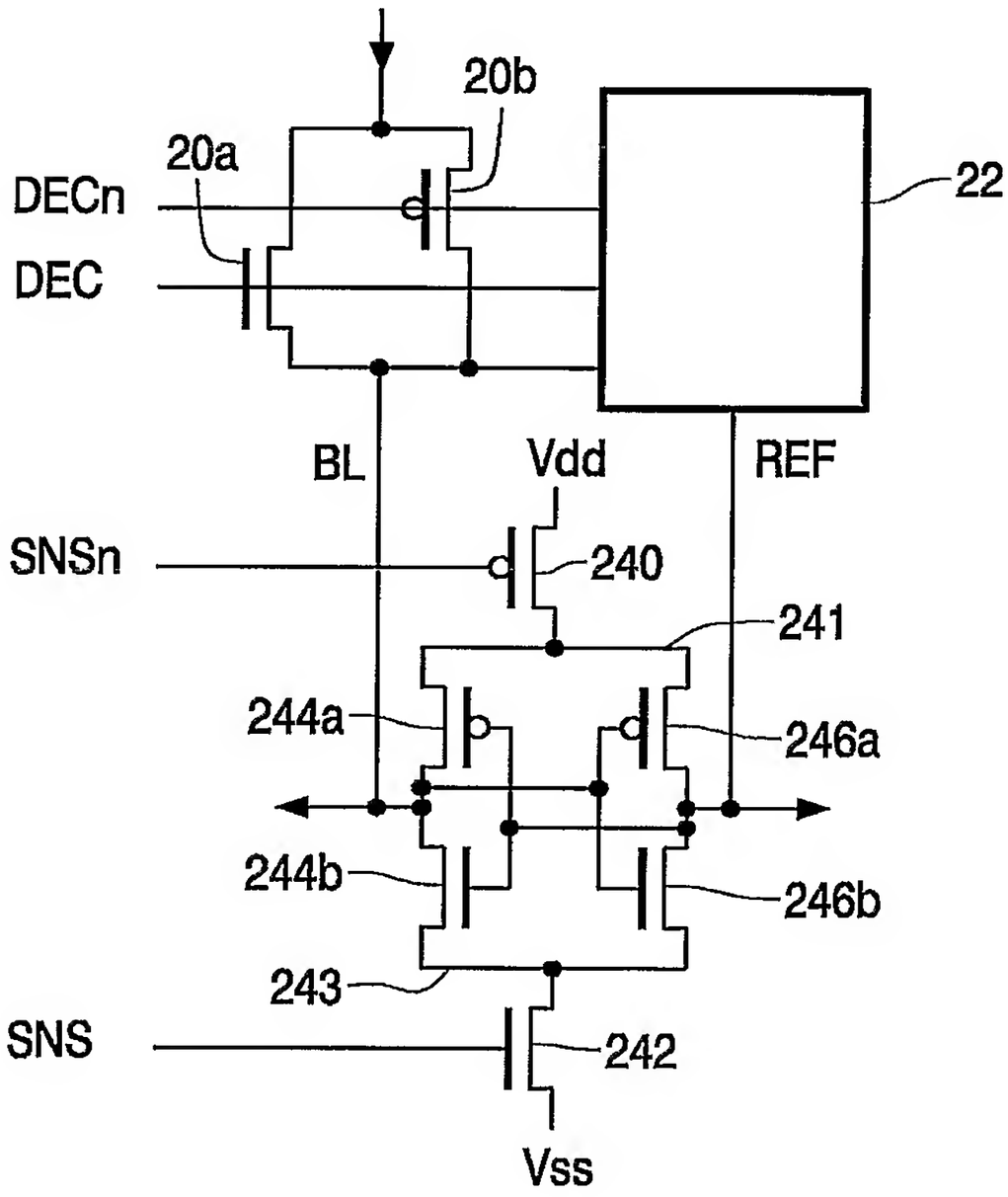
20b
20a
DECn
DEC
22
BL
Vdd
REF
SNSn
240
241
244a
246a
244b
246b
243
SNS
242
Vss

FIG. 2

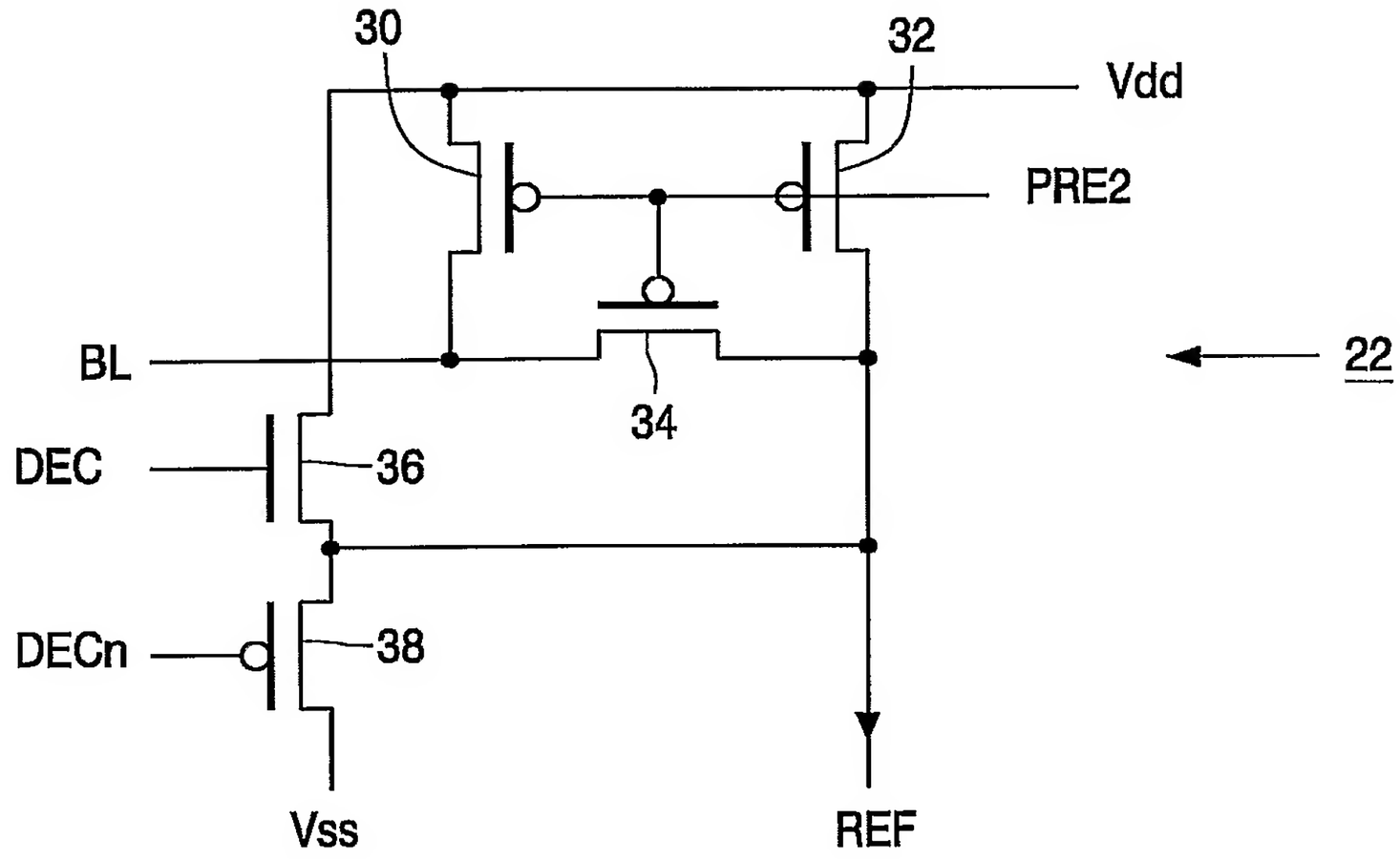
30
32
Vdd
PRE2
BL
22
34
DEC
36
DECn
38
Vss
REF

FIG. 3

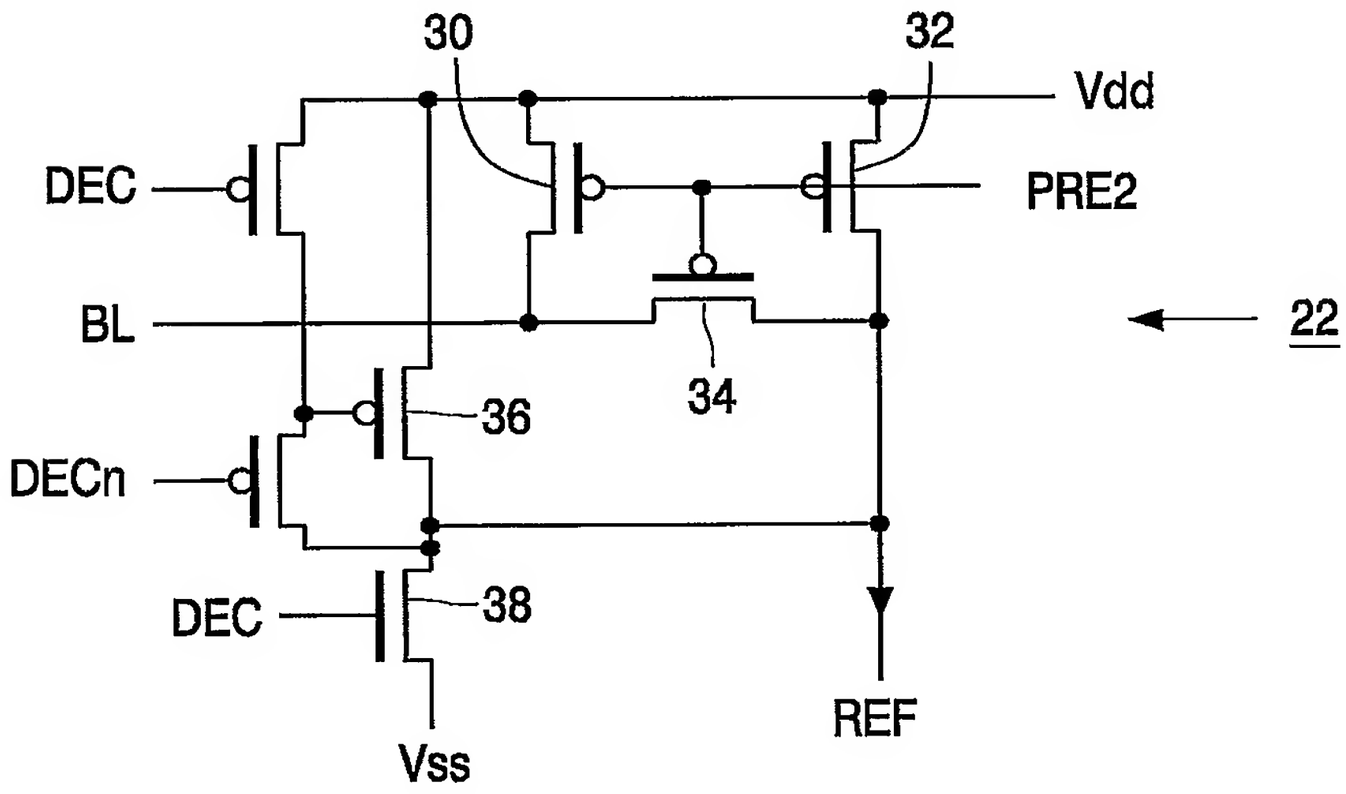
30
32
Vdd
DEC
PRE2
BL
22
34
36
DECn
DEC
38
REF
Vss

FIG. 3a

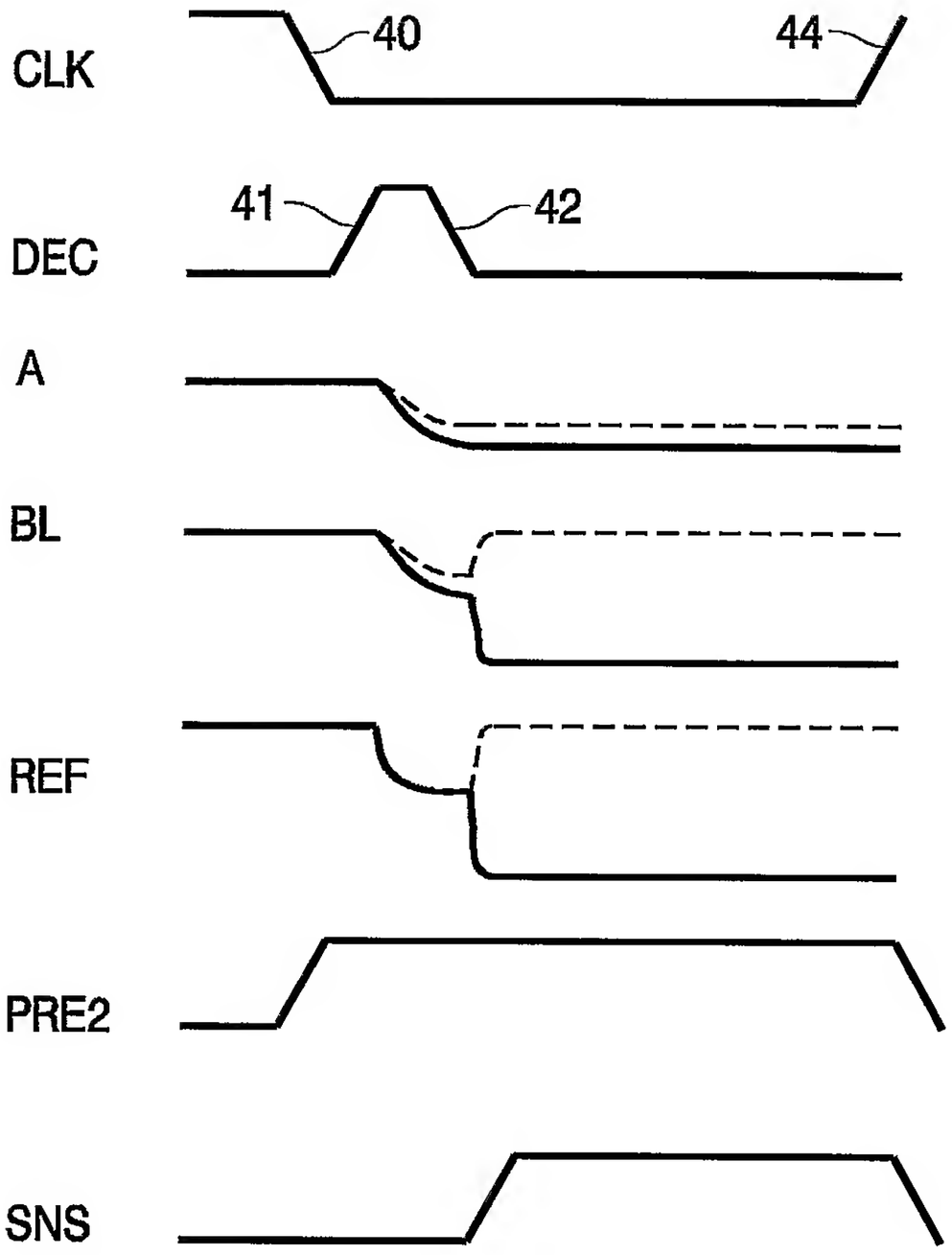

FIG. 4